

# 74ABT125

Quad buffer; 3-state

Rev. 3 — 29 April 2008

Product data sheet

## 1. General description

The 74ABT125 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ( $\overline{1OE}$ ,  $\overline{2OE}$ ,  $\overline{3OE}$ ,  $\overline{4OE}$ ), each controlling one of the 3-state outputs.

## 2. Features

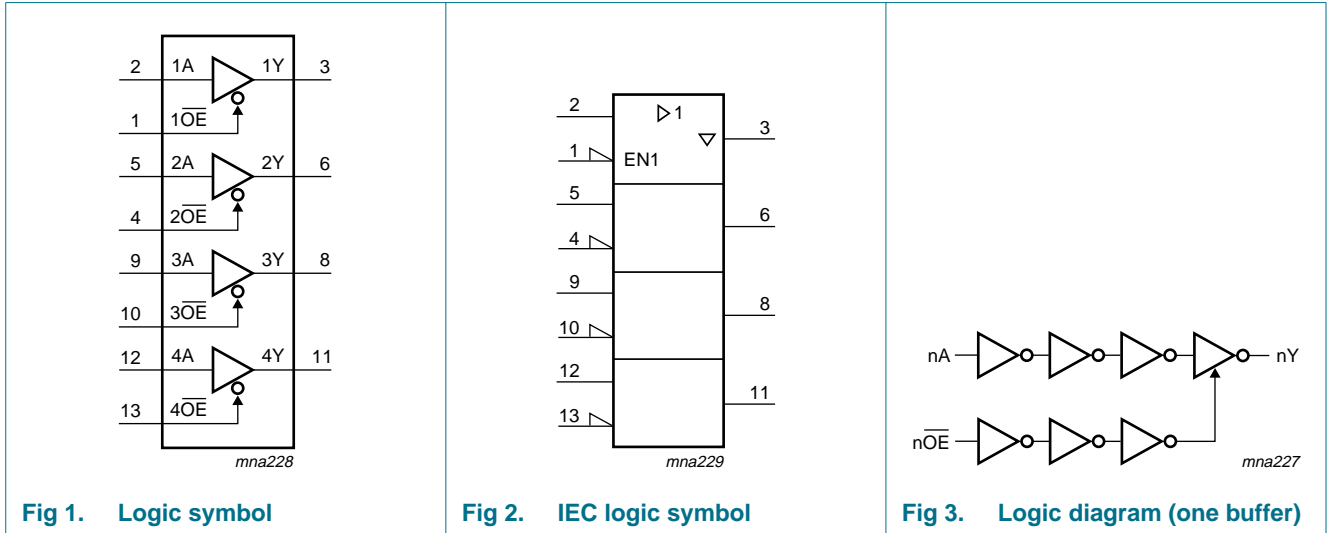
- Quad bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: HIGH -32 mA; LOW +64 mA
- Power-up 3-state
- inputs are disabled during 3-state mode
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

## 3. Ordering information

Table 1. Ordering information

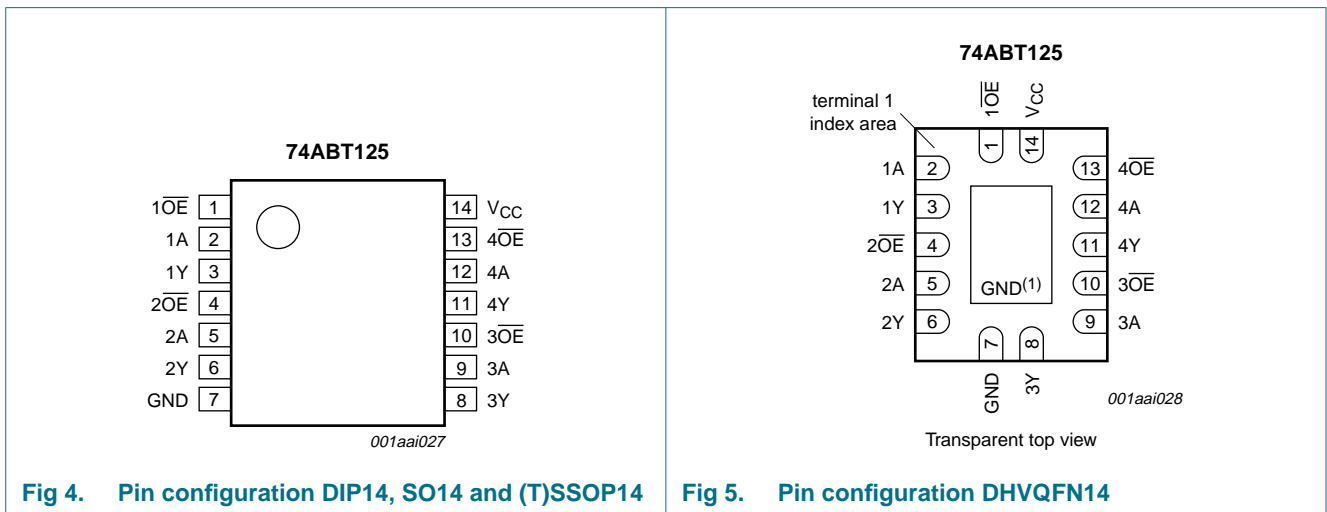
Type number	Package			
	Temperature range	Name	Description	Version
74ABT125N	-40 °C to +85 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74ABT125D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT125DB	-40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74ABT125PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ABT125BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram



### 5. Pinning information

#### 5.1 Pinning



#### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE to 4OE	1, 4, 10, 13	output enable input (active LOW)
1A to 4A	2, 5, 9, 12	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
VCC	14	supply voltage

## 6. Functional description

**Table 3. Function selection<sup>[1]</sup>**

Inputs		Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values<sup>[1]</sup>**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-1.2	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
T <sub>j</sub>	junction temperature		<sup>[2]</sup> -	150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	<sup>[3]</sup> -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
 For SSOP14 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	5.5	V
V <sub>I</sub>	input voltage		0	V <sub>CC</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	V
V <sub>IL</sub>	LOW-level Input voltage		-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-32	-	mA
I <sub>OL</sub>	LOW-level output current		-	64	mA
Δt/ΔV	input transition rise and fall rate		-	10	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-0.9	-1.2	-	-1.2	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>							
		V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -3 mA	2.5	2.9	-	2.5	-	V	
		V <sub>CC</sub> = 5.0 V; I <sub>OH</sub> = -3 mA	3.0	3.4	-	3.0	-	V	
		V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -32 mA	2.0	2.4	-	2.0	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 64 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	0.35	0.55	-	0.55	V	
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	µA	
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0.0 V; V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	-	±5.0	±100	-	±100	µA	
I <sub>O(pu/pd)</sub>	power-up/power-down output current	V <sub>CC</sub> = 2.1 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; $\overline{OE}$ = don't care	[1]	±5.0	±50	-	±50	µA	
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>							
		V <sub>O</sub> = 2.7 V	-	1.0	50	-	50	µA	
		V <sub>O</sub> = 0.5 V	-	-1.0	-50	-	-50	µA	
I <sub>LO</sub>	output leakage current	HIGH-state; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	5.0	50	-	50	µA	
I <sub>O</sub>	output current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V	[2]	-50	-100	-180	-50	-180	mA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>							
		outputs HIGH-state	-	65	250	-	250	µA	
		outputs LOW-state	-	12	15	-	30	mA	
		outputs disabled	-	65	250	-	50	µA	
ΔI <sub>CC</sub>	additional supply current	per control pin; V <sub>CC</sub> = 5.5 V; one control input at 3.4 V, other inputs at V <sub>CC</sub> or GND	[3]						
		outputs enabled	-	0.5	1.5	-	1.5	mA	
		outputs disabled	-	50	250	-	250	mA	
		one enable input at 3.4 V and other inputs at V <sub>CC</sub> or GND; outputs disabled	-	0.5	1.5	-	1.5	mA	
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	4	-	-	-	pF	
C <sub>O</sub>	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>	-	7	-	-	-	pF	

[1] This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 ms. From V<sub>CC</sub> = 2.1 V to V<sub>CC</sub> = 5 V ± 10 %, a transition time of up to 100 ms is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

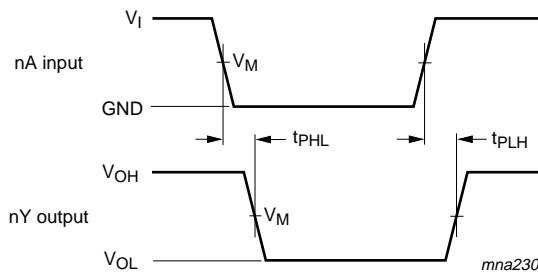
[3] This is the increase in supply current for each input at 3.4 V.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V. For test circuit, see Figure 8.*

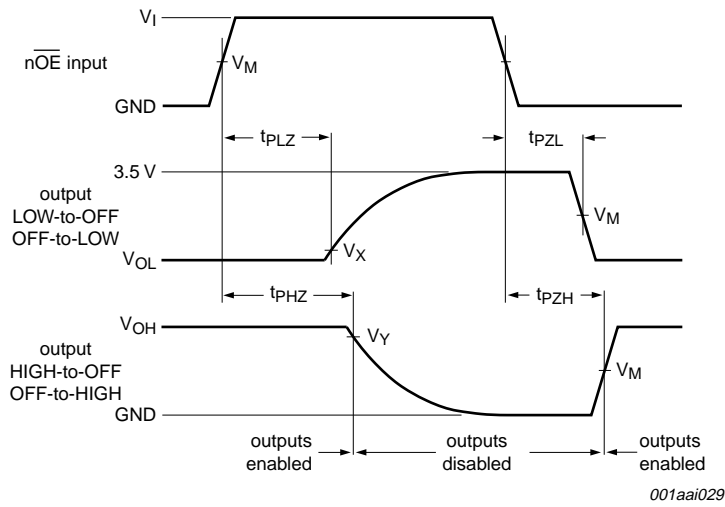
Symbol	Parameter	Conditions	25 °C; V <sub>CC</sub> = 5.0 V			-40 °C to +85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA to nY; see Figure 6	1.0	2.8	4.1	1.0	4.6	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA to nY; see Figure 6	1.0	3.1	4.6	1.0	4.9	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\overline{OE}$ to nY; see Figure 7	1.0	3.2	5.0	1.0	5.9	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\overline{OE}$ to nY; see Figure 7	1.0	4.2	6.2	1.0	6.8	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{OE}$ to nY; see Figure 7	1.0	4.1	5.4	1.0	6.2	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{OE}$ to nY; see Figure 7	1.5	2.8	5.0	1.5	5.5	ns

## 11. Waveforms



Measurement points are given in Table 8.  
 V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay input (nA) to output (nY)**

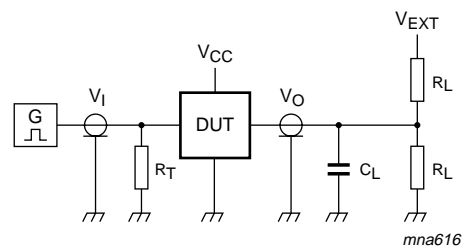
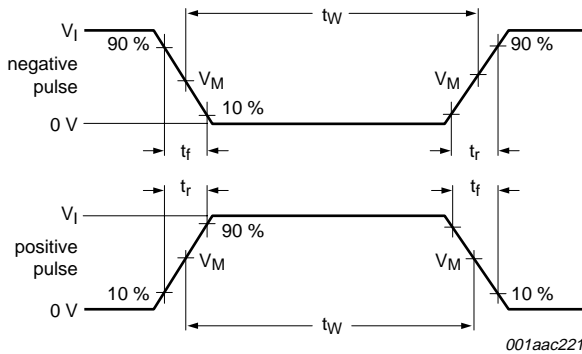


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 8. Measurement points**

Input		Output	
$V_I$	$V_M$	$V_X$	$V_Y$
3.0 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



a. Input pulse definition

b. Test circuit

Test data and  $V_{EXT}$  levels are given in [Table 9](#).  
 $C_L$  = Load capacitance including jig and probe capacitance.

**Fig 8. Test setup for switching times**

**Table 9. Test data**

Input	Load		$V_{EXT}$		
$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	open	open	7.0 V

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

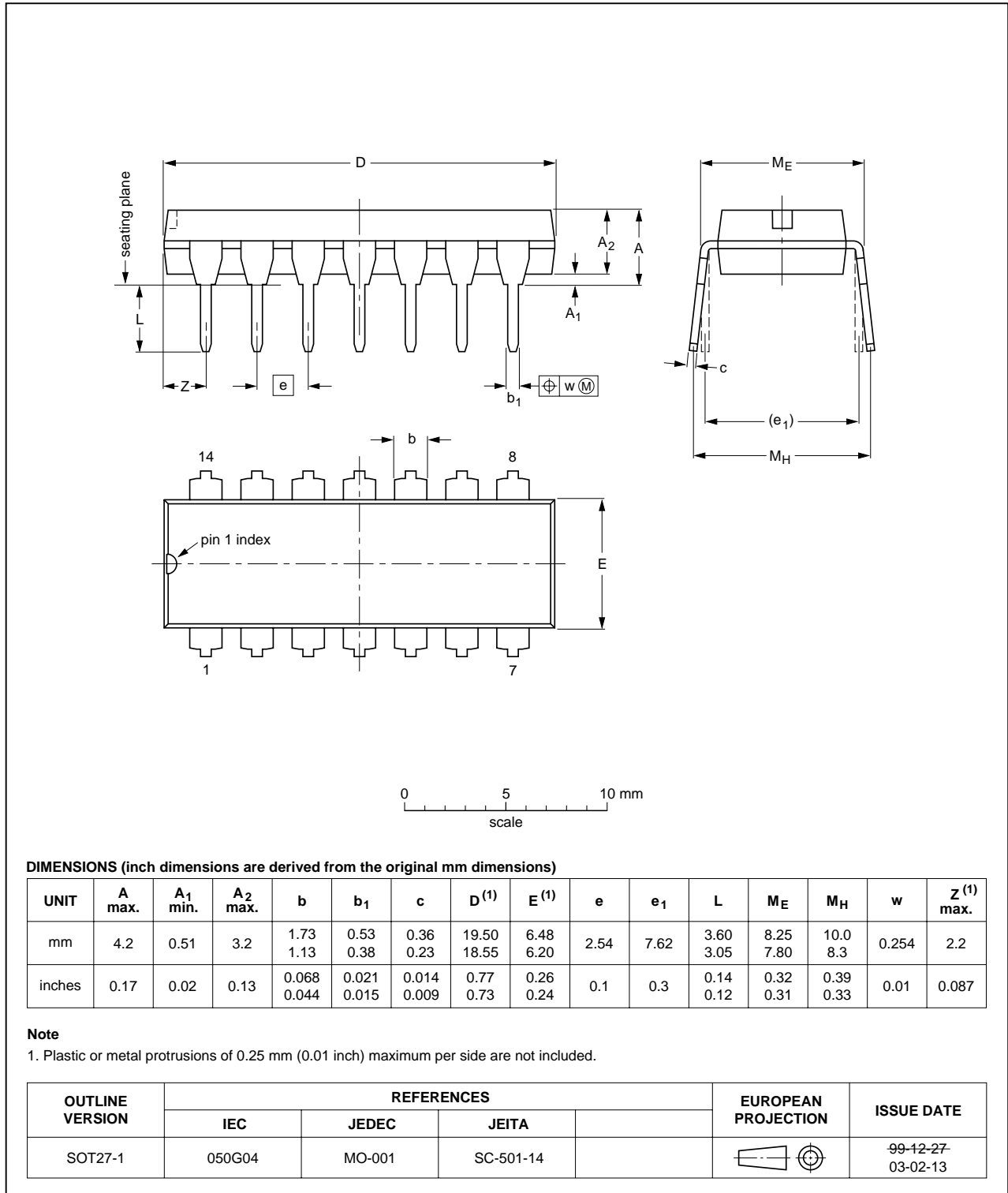


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

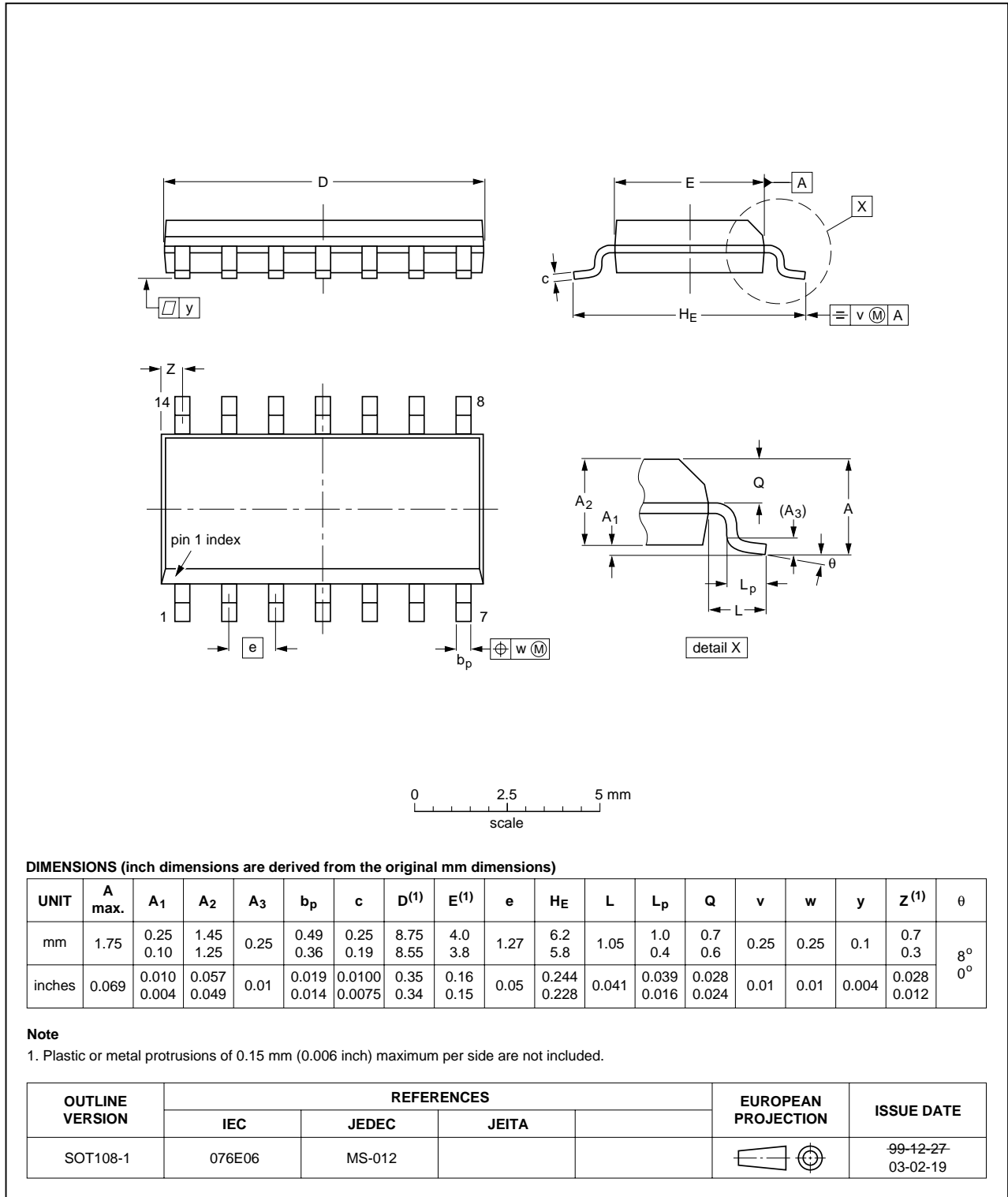


Fig 10. Package outline SOT108-1 (SO14)



SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

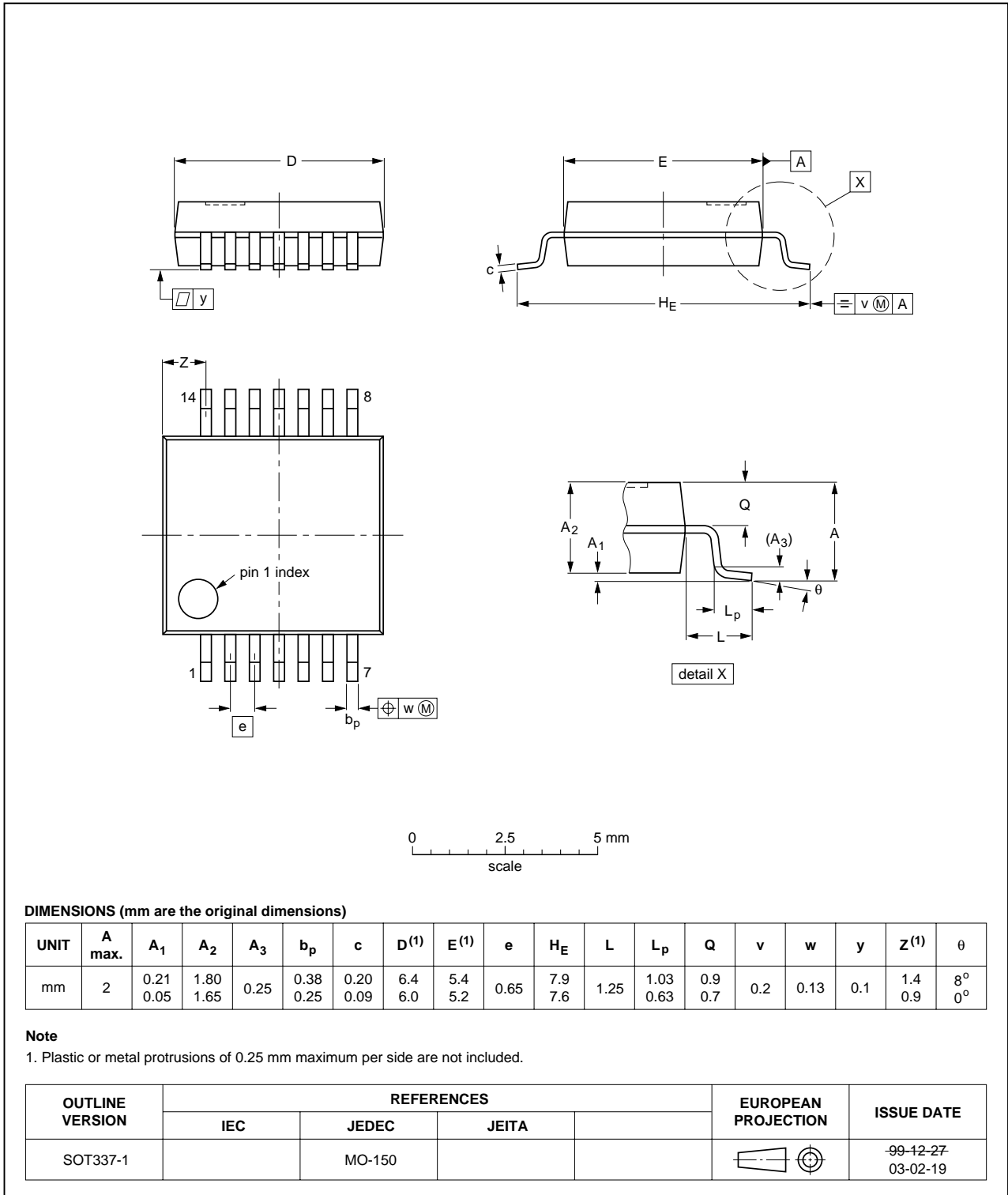


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

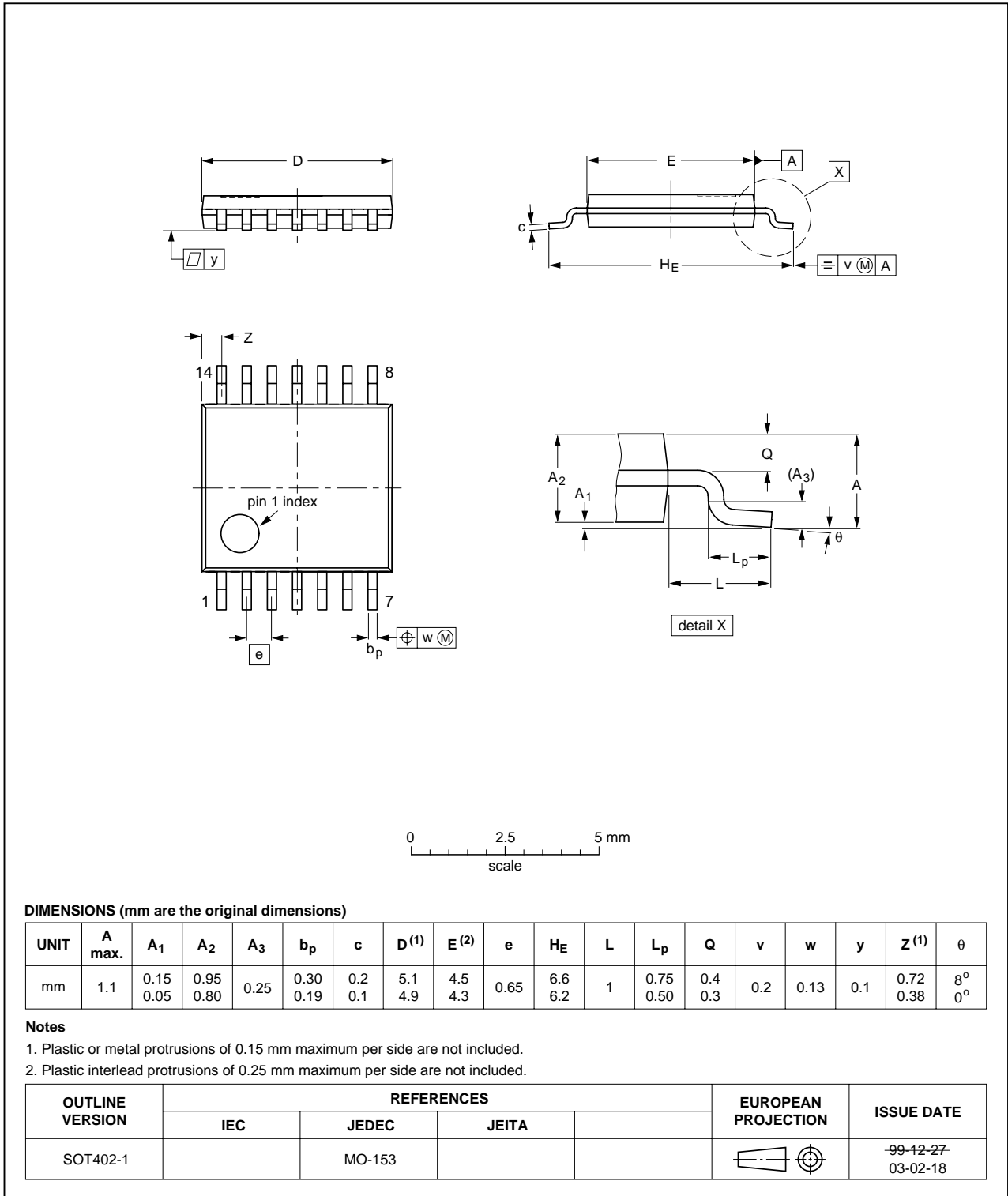


Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

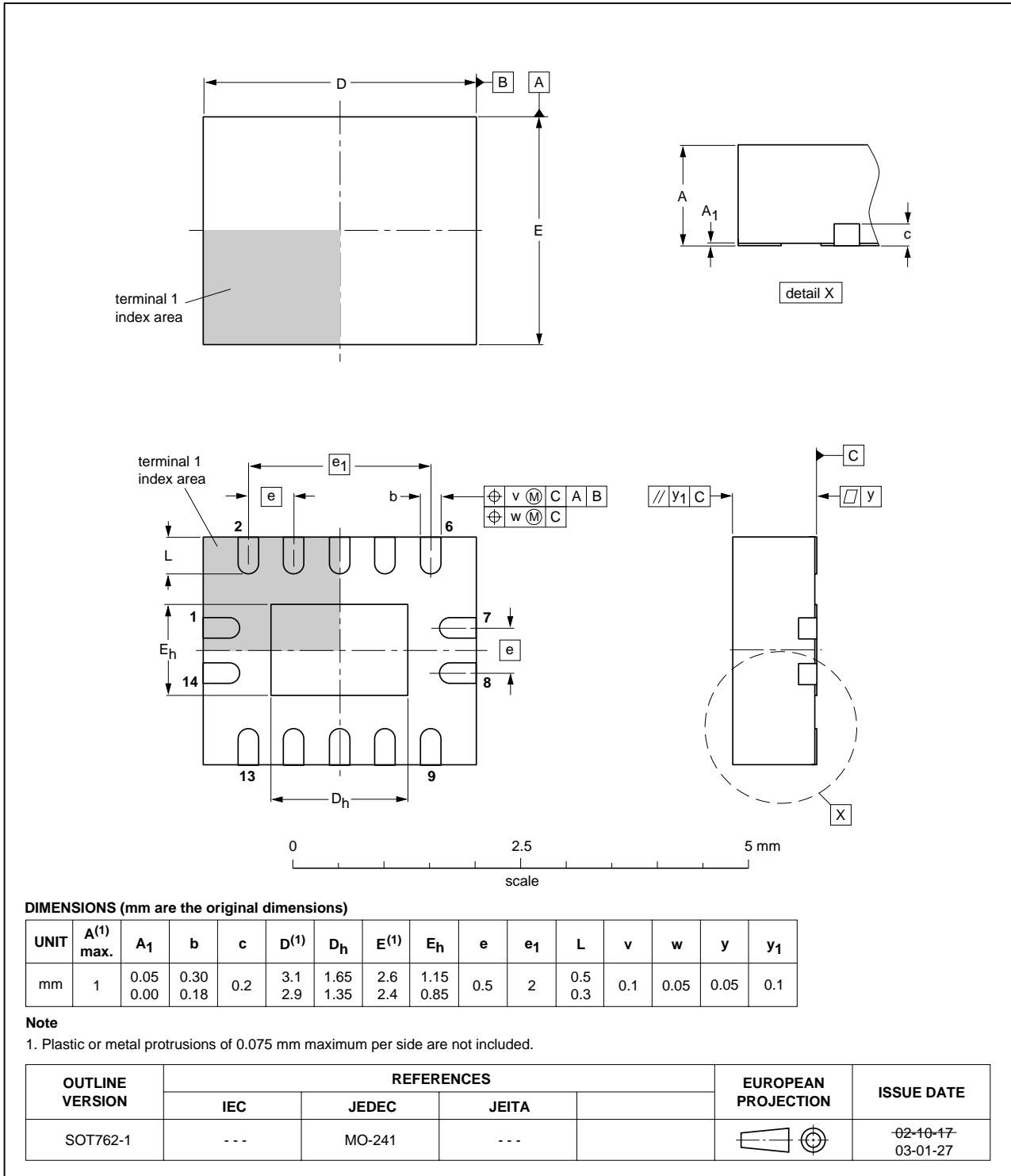


Fig 13. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bi-polarCMOS
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT125_3	20080429	Product data sheet	-	74ABT125_2
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Pins renamed throughout the data sheet.</li> <li>Package DHVQFN14 added to <a href="#">Section 3 “Ordering information”</a> and <a href="#">Section 12 “Package outline”</a>.</li> <li><a href="#">Figure 3 “Logic diagram (one buffer)”</a> added to <a href="#">Section 4 “Functional diagram”</a>.</li> <li><a href="#">Table 8 “Measurement points”</a> and <a href="#">Table 9 “Test data”</a> added.</li> <li><a href="#">Figure 8 “Test setup for switching times”</a> updated.</li> <li><a href="#">Section 13 “Abbreviations”</a> added.</li> </ul>		
74ABT125_2	19980116	Product specification	-	74ABT125_1
74ABT125_1	19960305	-	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 15.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

**17. Contents**

1 **General description** ..... 1

2 **Features** ..... 1

3 **Ordering information** ..... 1

4 **Functional diagram** ..... 2

5 **Pinning information** ..... 2

5.1 Pinning ..... 2

5.2 Pin description ..... 2

6 **Functional description** ..... 3

7 **Limiting values** ..... 3

8 **Recommended operating conditions** ..... 3

9 **Static characteristics** ..... 4

10 **Dynamic characteristics** ..... 5

11 **Waveforms** ..... 5

12 **Package outline** ..... 7

13 **Abbreviations** ..... 12

14 **Revision history** ..... 12

15 **Legal information** ..... 13

15.1 Data sheet status ..... 13

15.2 Definitions ..... 13

15.3 Disclaimers ..... 13

15.4 Trademarks ..... 13

16 **Contact information** ..... 13

17 **Contents** ..... 14

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 29 April 2008

Document identifier: 74ABT125\_3